CHAPTER 3

# Module Configuration

## 3.1 CPU Modules

The DRB1 processor/cache/memory subsystem provides an estimated benchmark of 20 SPECint95 and 21 SPECfp95, when operating at 400 MHz, with 256KBytes of internal 4-way associative cache and an industry-standard PC100 SDRAM memory controller.

The 370-pin CPGA CPU package is designed to plug into the CPU module connector on the Ultra AXI Systemboard and intended for early access customer development using the AXi Systemboard.

The DRB1 module is designed to plug into the CPU module connector on the Ultra AXI Systemboard and intended for early access customer development using the AXi Systemboard.

The DRB1 module has four General Purpose Outputs (GPOs) wired to J0301, as given in TABLE 3-1.

**TABLE 3-1** GPO Header J0301

| Pin 1 | Pin 2 | Pin 3 | Pin 4 | Pin 5 |
|---|---|---|---|---|
| GPO_3 | GPO_2 | GPO_1 | GPO_0 | GND |

FIGURE 3-1 illustrates the location of the DRB1 module components.

**Note –** Refer to the DRB1 Product Status document for revision and special operating information.

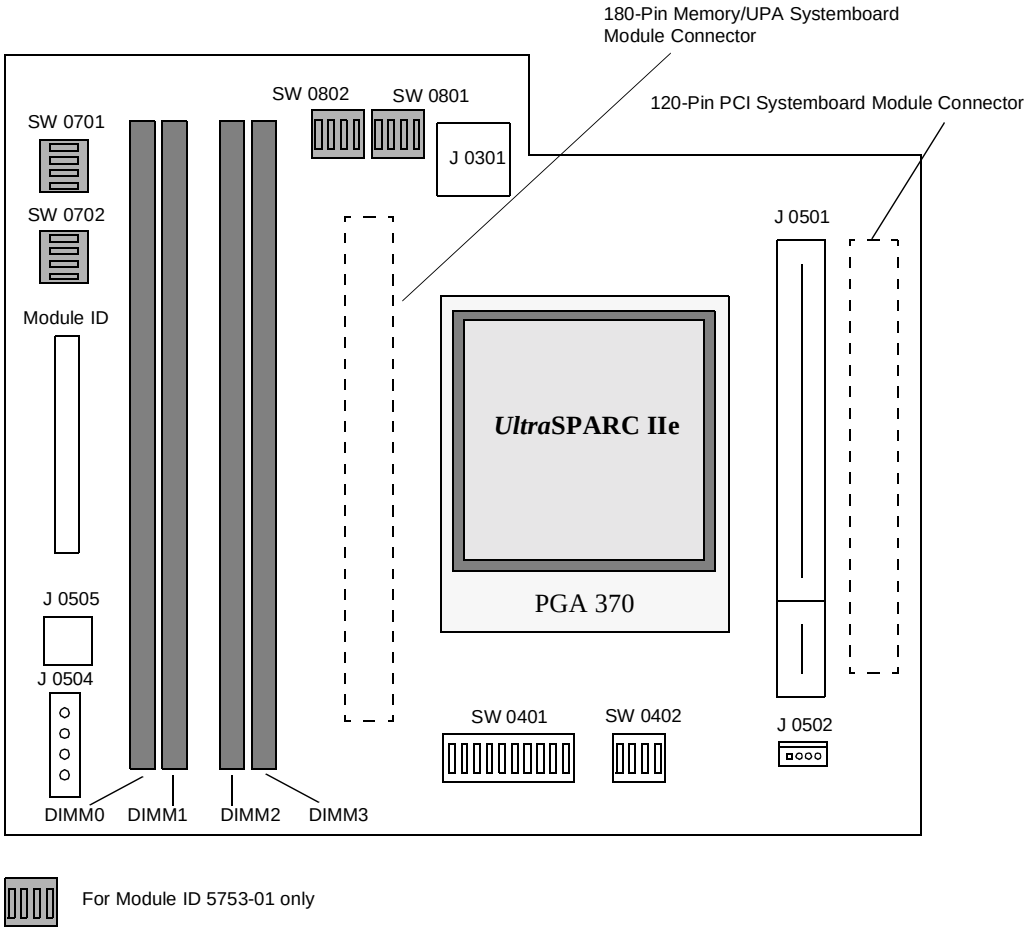


**FIGURE 3-1** DRB1 Module Component Location Diagram

# 3.2 Clock Frequency Settings

The clock speed is programmable via SW 04 01. The SW 04 01 is the last switch on the module PCB and is the only 10-position switch. This switch controls the CPU clock speed. The board is shipped from the factory set to 404MHZ.

The two Motorola 12429 switch speed settings for a VCO divide-by-2 for the system clock are given in TABLE 3-2. The location SW 04 02 switch setting determines by what rate the output module is divided. This setting will not change unless you prefer to run the DRB1 at a low speed. It is recommended to leave it at this setting.

For additional information on the clock chip, refer to the data sheet for the 12429 at:

`http://www.mot-sps.com/books/br1333/pdf/mc12429rev5.pdf`

You can use any clock chip capable of generating a 200 - 300MHz differential clock.

**TABLE 3-2** System Clock VCO Switch Settings (SW 04 02)

| Divide By | Position 1 (N1) | Position 2 (N0) | Position 3 | Position 4 |
|---|---|---|---|---|
| 2 | CLOSED | CLOSED (recommended setting) | NA | NA |
| 4 | CLOSED | OPEN | NA | NA |
| 8 | OPEN | CLOSED | NA | NA |
| 16 | OPEN | OPEN | NA | NA |

Loop divider values are given in TABLE 3-3. The values assume SW 02 04 Positions 1 and 2 are CLOSED.

**TABLE 3-3** Loop Divider Values (SW 04 01)

| Switch Position | 400MHZ | 426MHZ | 450MHZ | 470MHZ | 500MHZ |
|---|---|---|---|---|---|
| 1 = 1 (m0) | CLOSED | OPEN | OPEN | OPEN | CLOSED |
| 2 = 2 (m1) | CLOSED | CLOSED | CLOSED | OPEN | OPEN |
| 3 = 4 (m2) | CLOSED | OPEN | CLOSED | CLOSED | CLOSED |
| 4 = 8 (m3) | OPEN | CLOSED | CLOSED | OPEN | OPEN |
| 5 = 16 (m4) | CLOSED | OPEN | CLOSED | CLOSED | OPEN |
| 6 = 32 (m5) | CLOSED | CLOSED | OPEN | OPEN | OPEN |

**TABLE 3-3** Loop Divider Values (SW 04 01) *(Continued)*

| Switch Position | 400MHZ | 426MHZ | 450MHZ | 470MHZ | 500MHZ |
|---|---|---|---|---|---|
| 7 = 64 (m6) | OPEN | OPEN | OPEN | OPEN | OPEN |
| 8 = 128 (m7) | OPEN | OPEN | OPEN | OPEN | OPEN |
| 9 = 256 (m8) | CLOSED | CLOSED | CLOSED | CLOSED | CLOSED |

Make the SW0402 switch settings as follows:

- **SW0402 position 1**—set N1 bit of divider; setting from factory **CLOSED**.
- **SW0402 position 2**—set N0 bit of divider, setting from factory **CLOSED**.
- **SW0402 position 3**—set SYNC_3to1 signal bit; setting from factory **OPEN**.

  SW0402 position 3 is used to set how many synchronizers are used between the CPU and PCI clock domains. **OPEN** = 2 synchronizers; **CLOSED** = 3 synchronizers. This bit is usually set to 2 or **OPEN**.

To get 400MHz from the CPU, it must be feed 200 MHz. The settings work only when in divide-by-2 mode, and when in this mode, the frequency out is the added binary value of the nine inputs of the clock chip. The least significant bit is 1 (at SW0401 switch 1) to 256 at switch nine of SW0401.

The PC100 memory bus speed is determined in **<<OBP version x.x.x>>** by dividing the CPU speed, as follows:

- If the CPU speed is 400MHZ or less, then the PC100 speed is calculated as the CPU frequency divided by four.
- If the CPU speed is 400MHZ or less, then the PC100 speed is calculated as the CPU frequency divided by four.
- If the CPU speed is 500MHZ or less, then the PC100 speed is calculated as the CPU frequency divided by five. For example, if the CPU frequency = 408MHZ, then the PC100 bus is 408 / 5 = 81.6MHZ.

# 3.3 $1^2$C Bus Connection

The PC100 DIMMs use the $I^2C$ system bus to communicate their size, location, and other data required for the CPU firmware to setup memory control.

The DRB1 $I^2C$ cable is soldered directly to J0703 and connects to the AXi I2C header on the Systemboard at J3601. Pin 1 of this header points away from J0601. The DIMM addresses can be set to any of eight addresses. The factory sets the addresses as:

J0701 = 0, J0702 = 1, J0801 = 2, J0802 = 3.

**Note –** The DIMM address settings are specific to the revision.

# 3.4 SDRAM DIMM Installation and Switch Settings

Silicon Revision 1.1 is limited to using a single 128-Mb DIMM **<<what is the part number?>>**. Revision 1.2 has been successfully tested with approximately 10 types. Contact Sun Microsystems if you want to use DIMMs other than what is shipped with the system.

When the DRB1 PROM image is present for the IIe module, and the jumpers are set correctly, you can now set the module switches.

## 3.4.1 Preparing the Switches

The memory $I^2C$ address switch settings are given in TABLE 3-7. These settings define address settings for each switch. You may set the addresses of the DIMMs different from the settings given, but the PROM to reflect the different settings. $I^2C$ addresses can be individually set from 0 - 7. When you open a position, you define a one for that bit. Each switch uses only the first three positions.

**Note –** These switches are not included on the DRB1 module with part number 270-5753-02.

**TABLE 3-4** SW0701, SW0702, SW0801, and SW0802 Switch Settings (5753-01 rev. only)

| Address Value | Bit 2 | Bit 1 | Bit 0 | Default |
|---|---|---|---|---|
| 0 | CLOSED | CLOSED | CLOSED | SW0701(DIMM0) |
| 1 | CLOSED | CLOSED | OPEN | SW0702 (DIMM1) |
| 2 | CLOSED | OPEN | CLOSED | SW0801 (DIMM2) |
| 3 | CLOSED | OPEN | OPEN | SW0802 (DIMM3) |
| 4 | OPEN | CLOSED | CLOSED | |

**TABLE 3-4** SW0701, SW0702, SW0801, and SW0802 Switch Settings (5753-01 rev. only)

| Address Value | Bit 2 | Bit 1 | Bit 0 | Default |
|---|---|---|---|---|
| 5 | OPEN | CLOSED | OPEN | |
| 6 | OPEN | OPEN | CLOSED | |
| 7 | OPEN | OPEN | OPEN | |

# 3.5 Cooling

Both modules are cooled by a heat sink with an integral 12-volt fan that receives power through a cable wired to J0505. The Systemboard heat sink fan header pinouts are given in TABLE 3-2 and TABLE 3-3. Power for the Systemboard heat sink comes via an extra power connector from the ATX power supply. The chassis must also have a fan to replace the air surrounding the module.

**TABLE 3-5** J0504 CPU Heat Sink Fan Header on the AXi Systemboard

| Pin # | Signal Name | Pin # | Signal Name |
|---|---|---|---|
| 1 | +12VDC | 2 | Ground |
| 3 | Ground | 4 | +5VDC |

**TABLE 3-6** J0505 CPU Heat Sink Fan Header on the AXi Systemboard

| Pin # | Signal Name | Pin # | Signal Name |
|---|---|---|---|
| 1 | Ground | 2 | +12VDC |
| 3 | Ground | | |

# 3.6 Module Connectors

Refer to Appendix A, PROM Emulator and Flash Update Procedure, and Pin Assignments, for a complete listing of module connections.

# 3.7 PCI Bus Slot

The DRB1 provides a 32-bit, 33 or 66MHZ 2.1 PCI bus. The module's configuration is for 66MHZ. TheJ0601 connector mates to the Systemboard and drives the Advanced PCI Bridge (APB) chip on the Systemboard. An industry-standard 32-bit 66MHZ, 3.3VDC PCI slave connector, with no interrupts, is on the module at J0501. A 4-pin header is wired to the PCI interrupt pins. This header can be used to provide interrupts to the slot.

Refer to Appendix A, Pinouts and Connections, for the complete lists of 120-Pin J0601 system PCI connections and J0501 32-bit 66MHz Slave PCI slot connections.

## 3.7.1 Setting the Module Switches

When the DRB1 PROM image is present for the IIe module, and the jumpers are set correctly, you can now set the module switches.

### 3.7.1.1 Preparing the Switches

The memory I2C address switch settings are given in TABLE 3-7. These settings define address settings for each switch. You may set the addresses of the DIMMs different from the settings given, but the PROM to reflect the different settings. I2C addresses can be individually set from 0 - 7. When you open a position, you define a one for that bit. Each switch uses only the first three positions.

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**Note –** These switches are not included on the DRB1 module with part number 270-5753-02.

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**TABLE 3-7** SW0701, SW0702, SW0801, and SW08002 Switch Settings

| Address Value | Bit 2 | Bit 1 | Bit 0 | Default |
|---|---|---|---|---|
| 0 | CLOSED | CLOSED | CLOSED | DIMM0 |
| 1 | CLOSED | CLOSED | OPEN | DIMM1 |
| 2 | CLOSED | OPEN | CLOSED | DIMM2 |
| 3 | CLOSED | OPEN | OPEN | DIMM3 |
| 4 | OPEN | CLOSED | CLOSED | |

**TABLE 3-7** SW0701, SW0702, SW0801, and SW08002 Switch Settings *(Continued)*

| Address Value | Bit 2 | Bit 1 | Bit 0 | Default |
|---|---|---|---|---|
| 5 | OPEN | CLOSED | OPEN | |
| 6 | OPEN | OPEN | CLOSED | |
| 7 | OPEN | OPEN | OPEN | |